**CLAIMS:**

1. An interface apparatus comprising:

a processor for receiving at least one Network Interface signal, and for recognizing a transport mechanism associated with each Network Interface signal; and

a bus interface device for generating at least one System Interface signal in response to the recognized transport mechanism.

2. The interface apparatus of Claim 1, wherein the transport mechanism comprises at least one of Asynchronous Transfer Mode, Internet Protocol, Frame Relay, Integrated Services Digital Network, High bit-rate Digital Subscriber Line, Asymmetric Digital Subscriber Line, Very High Data Rate Digital Subscriber Line, Symmetric Digital Subscriber Line, 10 base T, 100 base T, Gigabit Ethernet and E1/T1.

3. The interface apparatus of Claim 2, wherein the processor recognizes the transport mechanism for each Network Interface signal in response to a control signal.

4. The interface apparatus of Claim 2, wherein the processor further examines a pattern for each Network Interface signal to recognize the associated transport mechanism.

5. The interface apparatus of Claim 4, wherein each System Interface signal is coupled with at least one of a circuit switched interface, a packet switched interface, and a combined circuit packet switched interface.

6. The interface apparatus of Claim 5, wherein the transport mechanism comprises an adaptation layer of Asynchronous Transfer Mode, the processor performs ATM adaptation layer processing on each Network Interface signal in response to the recognized transport mechanism.

7. The interface apparatus of Claim 6, wherein at least one the processor and the bus interface device matches a timing of the circuit switched interface and formats the ATM adaptation layer processed Network Interface signal to the corresponding System Interface signal.

8. The interface apparatus of Claim 7, comprising a control switch for partitioning and switching the performance of the matching the timing and the performance of the formatting the ATM adaptation layer processed Network Interface signal between the processor and the bus interface device in response to a control signal.

9. The interface apparatus of Claim 5, wherein at least one the processor and the bus interface device converts each Network Interface signal to correspond with the packet switched interface and routes each converted Network Interface signal.

**10.** The interface apparatus of Claim **9**, comprising a control switch for partitioning and switching the performance of the converting each Network Interface signal and the routing each converted Network Interface signal in response to a control signal between the processor and the bus interface device.

**11.** The interface apparatus of Claim **5**, comprising means for coupling the processor with the bus interface device, the means for coupling comprising at least one of a serial bus, a parallel bus and shared memory.

**12.** The interface apparatus of Claim **5**, wherein the processor performs a traffic management on each Network Interface signal.

**13.** The interface apparatus of Claim **5**, wherein the processor receives each Network Interface signal from a physical layer input bus device for supporting at least one of an electro- and an opto- scheme.

**14.** The interface apparatus of Claim **5**, wherein the processor comprises at least one of a field programmable gate array, an application specific integrated circuit, a digital signal processor, a controller and a special purpose processor.

15. The interface apparatus of Claim 5, wherein the bus interface device comprises at least one programmable logic device for interfacing the processor with the at least one of a circuit switched interface, a packet switched interface, and a combined circuit packet switched interface.

16. The interface apparatus of Claim 5, wherein the bus interface device comprises:

a circuit switched interface device for buffering, data formatting, and timing resolution; and

a packet switched interface device for supporting protocol conversion, routing, and bus access.

17. The interface apparatus of Claim 5, wherein the bus interface device comprises:

a single interface device for buffering, data formatting, and timing resolution if circuit switched and for supporting protocol conversion, routing, and bus access if packet switched.

**18.** The interface apparatus of Claim **17**, wherein the single interface device supports at least one of a TDM bus and a Packet/Cell bus.

**19.** The interface apparatus of Claim **17**, wherein the single interface device comprises a programmable logic element.

**20.** The interface apparatus of Claim **17**, wherein the single interface device supports a dynamic bus allocation.